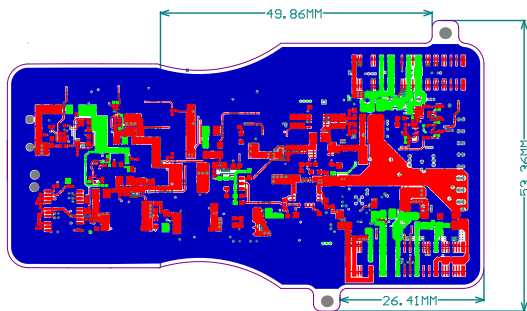


2271 ■ Install label in silkscreened box like (Fig. 10-2). Text shall be 8 pt font. Text shall be box the 7.8 mil. 7.1

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38  
ASSEMBLY VARIANT: [No Variations]

[illegible]

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Z23 ■ These assemblies must be covered by a silkscreen label with the following information. The label must be placed on the top of the assembly.					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	



1.FABRICATE PER IPC-6012A CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES.

19. BOARD DIMENSION: 90 MM X 53.36 MM.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TUNED EXCEPT ON PAD VIAS

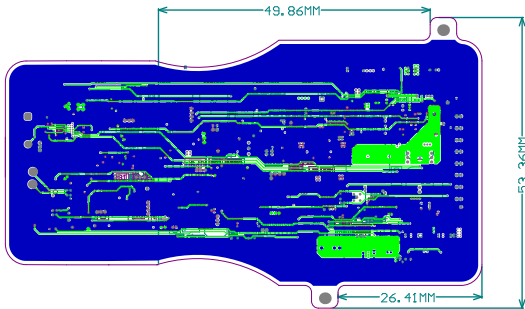
E

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1



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.38 TOM 01U0H8 '94M' 03XRAM 27H3049M03  
ASSEMBLY VARIANT: [No Variations] [noitsreV oM] :TVAIRAU YJBM322A

DESIGNED BY: Bill Xu	DATE: 9/18/2024	DESIGNED BY: Bill Xu	DATE: 9/18/2024
LAYER NAME = Top	TID #: 010269	LAYER NAME = Bottom	TID #: 010269
PLTNAME: TID010269	DATE: 9/18/2024	PLTNAME: TID010269	DATE: 9/18/2024

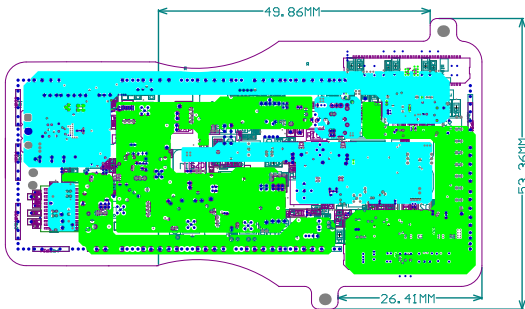
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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/-
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER
<input checked="" type="checkbox"/> MATTIE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENERPIG	
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay	Solder Resist	1.00mil	3.5	
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. ASSEMBLY VARIANT: [No Variations]

PCB: 010269	00	BOARD: 010269	00	SUN: 010269	00
LAYER NAME =	00	TID #: 010269	# 01T	010269	01
PLT: 010269	00	GENERATED: 9/18/2023	3:43:18 PM	TEXAS INSTRUMENTS	01

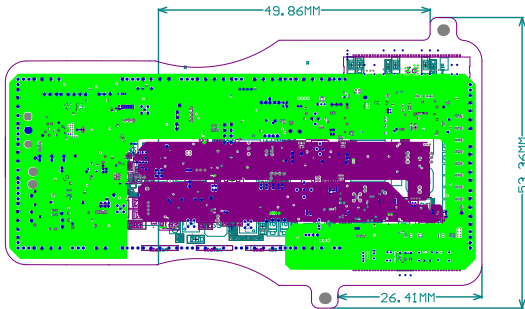
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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-	3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269_PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay	Solder Resist	1.00mil	3.5	
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL , 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL , 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. ASSEMBLY VARIANT: [No Variations]

REVISION: 00	DATE: 00	SUN 3/26/2018 3:43:20 PM	TEXAS INSTRUMENTS
LAYER NAME = Top	TID #: 0010A-010269	QIT	0010A-010269
PLT: 0010A-010269	GENERATED: 9/18/2018 3:43:20 PM	TEXAS INSTRUMENTS	

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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-	3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	


Z23 ■ These assemblies must be covered by a silkscreen label with the following information:					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	

1.FABRICATE PER IPC-6012N CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007" ) PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES.

19. BOARD DIMENSION: 90 MM X 53.36 MM.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TUNED EXCEPT ON PAD VIAS

 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269_PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill. Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31



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1	2	3	4	5	6
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Z23 ■ These assemblies must be covered by a top solder mask or a top solder mask with an acceptable solder mask coverage.					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	



1.FABRICATE PER IPC-6012A CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES.

16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38  
ASSEMBLY VARIANT: [No Variations]

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B

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-010269.PcbDoc

ENGINEER:  
Bill. Xu

SCALE: 1.00

LAYOUT BY:  
Bill.Xu

ALTium DESIGNER VERSION:  
24.9.1.31




221 ■ Install label in silkscreened box after final wash. Text shall be 9 pt font. Text shall be per the Label Table in the QIP schematic.

19. BOARD DIMENSION: 90 MM X 53.36 MM.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

[illegible]

 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE: Smart Probe Power Supply	
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FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31



Z23 ■ These assemblies must be covered by a silkscreen label with the following information:					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	


1.FABRICATE PER IPC-6012A CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES.

19. BOARD DIMENSION: 90 MM X 53.36 MM.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TENDED EXCEPT ON PAD VIAS

21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

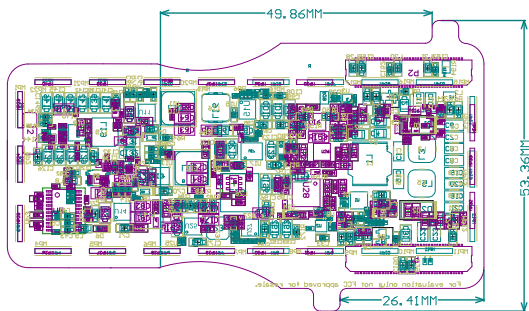
 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1:00	ALTIM DESIGNER VERSION: 24.9.1.31



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221 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the DDP schematic.

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31

ACB;AES;CBC;PADDING;ECPDDOTIAP;SEDE	00	BARD	#S:TIDA#01D269	DARE;	00	SUN;RED;NXTT8H	MORFION;JOUT;EDR
LAYER NAME = Mfr 3000 Superthin Topom	TID #: #S:TIDA#01D269 :# QIT		motto8 pldmezzaf dM				
PLOT NAME T:\Boxton Silkscreen Overlay.s	GENERATED \e : 9/19/2024/13		3:45:35 PM	nne9c3x;lz	TEXAS INSTRUMENTS .JP		

Z23 ■ These assemblies must be covered by a silkscreen label with the following information:					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	

1.FABRICATE PER IPC-6012N CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007" ) PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES.

19. BOARD DIMENSION: 90 MM X 53.36 MM.


20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TUNED EXCEPT ON PAD VIAS

21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



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PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269_PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31



Z23 ■ These assemblies must be covered by a top solder mask or a top solder resist. The top solder mask or top solder resist must be applied to the top of the assembly.					
1	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.78mm	4.2	
2	GND1	CF-004	0.28mm		
2	Dielectric 2	PP-006	2.78mm	4.1	
3	Signal 1	CF-004	0.69mm		
Z22 ■ These assemblies are ESD sensitive because they are observed.					
2	Dielectric 3	PP-006	2.78mm	4.1	
4	Power 1	CF-004	0.69mm		
4	Dielectric 4	PP-006	2.78mm	4.1	

1.FABRICATE PER IPC-6012A CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,

13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



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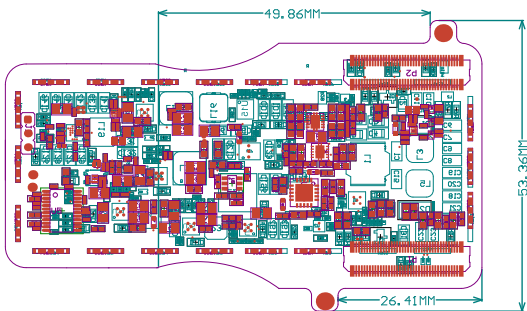


SCALE: 1.00	ALTUM DESIGNER VERSION: 24.9.1.31
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7271 ■ Install label in silkscreened box also. This label must show the following dimensions: 1.8 mm

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ) PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 0.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMASINIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



PAGE:	AESDDE	FILEIDPDDOITGPSEDE		00	BUPAD	E8S2TIDA#01D269	GAREB:	00	SUN DEE: NARTG	MORFISGSJGDHAE
LAYER NAME =	NIP	SourceRegionTopom	Bottom	TID #:	E8S2TIDA#01D269:#	DIT	mottoB	pIdmezaaR dM		
PLOT NAME TOI Top Solder Mask Print + : E & S	GENERATED \e :	9/18/2017 13:43:45 PM JeeM	ebljEXASTINSTRUMENTS\JA							

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**DESIGN INFORMATION**

MIN. TRACK WIDTH: 4 MIL  
MIN. CLEARANCE: 4.75 MIL  
MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL; HOLES +/- 3 MIL  
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**

☐ FR-408 ☐ FR-4 High Tg ☒ OTHER FR-4

THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER \_\_\_\_\_

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

**DRILLING:**

REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30  $\mu$ m ☐ OTHER \_\_\_\_\_

**BOARD FINISH:**

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER \_\_\_\_\_

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER \_\_\_\_\_  
☐ MATTE ☐ SEMI-GLOSS

**SURFACE FINISH:** ☒ IMMERSION GOLD (ENG) ☐ ENERPIC  
☐ MM. TIN/SILVER OR EQUIV ☐ OTHER \_\_\_\_\_

**ARRAY/PANEL:** ☒ CUT AND TRIM PER M1 BOARD OUTLINE  
☐ N.C. ROUTE ☐ V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs  
TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☐ RoHS ☐ OTHER PER ORDER \_\_\_\_\_

**ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.**  
**PCB MUST BEAR THE UL94V-0 UL CERTIFIED MATERIAL D NUMBER**

**ADDITIONAL REQUIREMENTS:**

MICROSECTION: ☐ YES ☐ NO

BASE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☒ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
☒ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
☐ TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE:  
Smart Probe Power Supply

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-010269.PcbDoc

ENGINEER:  
Bill. Xu

LAYOUT BY:  
Bill.Xu

ALTUM DESIGNER VERSION:  
24.9.1.31

Z23 ■ These assemblies must be covered with a clear plastic film to protect the components from moisture and corrosion.					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	



1.FABRICATE PER IPC-6012N CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,

19. BOARD DIMENSION: 90 MM X 53.36 MM.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TUNED EXCEPT ON PAD VIAS

LE



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1

Z23 ■ These assemblies must be covered by a silkscreen label with the following information:					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED  
ASSEMBLY VARIANT: [No Variations]

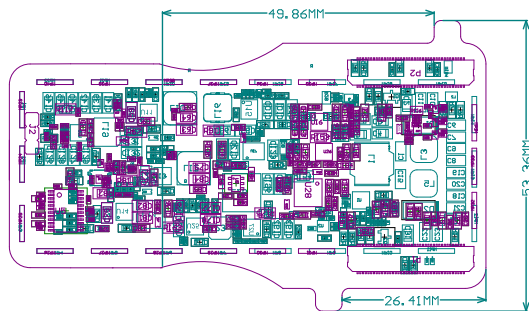
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- NOTES: (UNLESS OTHERWISE SPECIFIED)
- 1.FABRICATE PER IPC-6012A CLASS 2
  - 2.LAMINATE MATERIAL: FR4
  - 3.COPPER WEIGHT: SEE STACKUP
  - 4.BOARD THICKNESS: 1.6MM +/- 10%
  - 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
  - 6.SURFACE FINISH: ENIG
  - 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
  - 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
  - 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
  - 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
  - 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007" ) PER INCH AS MEASURED PER IPC-TM-650.
  - 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
  - 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
  - 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
  - 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
  16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
  17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
  18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
  19. BOARD DIMENSION: 90 MM X 53.36 MM.
  - 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMASINIG LAYERS WILL BE HALF OUNCE
  21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

C

221 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the


- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 36 COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
ASSEMBLY VARIANT: [No Variations] [Variations: 0]

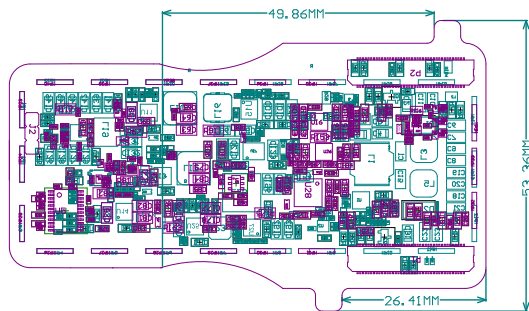
[illegible]

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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.75 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4
THICKNESS: <input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10%	<input type="checkbox"/> OTHER _____
TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	<input type="checkbox"/> OTHER +/- _____
BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	<input type="checkbox"/> OTHER +/- _____
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN	<input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um	<input type="checkbox"/> OTHER _____
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP	<input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE	<input type="checkbox"/> OTHER _____
SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN	<input type="checkbox"/> OTHER _____
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG)	
<input type="checkbox"/> IM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER _____
ARRAY/PANEL:	
<input checked="" type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE	<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input checked="" type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input checked="" type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL LAYERS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE:	
Smart Probe Power Supply	
DESIGNED FOR:	
Public Release	
FILE NAME:	
TIDA-010269.PcbDoc	
ENGINEER:	LAYOUT BY:
Bill. Xu	Bill. Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31

221 ■ Install label in silkscreened box after final wash. Text shall be 2 pt font. Text shall be per the Label Table in the

1. FABRICATE PER IPC-6012A CLASS 2
2. LAMINATE MATERIAL: FR4
3. COPPER WEIGHT: SEE STACKUP
4. BOARD THICKNESS: 1.6MM +/- 10%
5. NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
6. SURFACE FINISH: ENIG
7. SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
8. DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
9. SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR: GREEN
10. SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
11. BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
12. SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
13. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
14. ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
15. LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38 COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
ASSEMBLY VARIANT: [No Variations] ASSEMBLY VARIANT: [No Variations]

[illegible]

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**DESIGN INFORMATION**

MIN. TRACK WIDTH: 4 ML  
MIN. CLEARANCE: 4.75 ML  
MIN. VIA PAD SIZE: 12 ML  
MINIMUM ANNUAL RING 0.05mm (2ML) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C  
REGISTRATION TOLERANCES: METAL +/- 5 ML, HOLES +/- 3 ML  
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 ML

**MATERIAL:**  
☐ FR-408 ☐ FR-4 High Tg ☒ OTHER ☐ FR-4  
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER \_\_\_\_\_  
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_  
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

**DRILLING:**  
REFERENCE: ☒ AS SHOWN ☒ NC DRILL FILES  
PTH COPPER THICKNESS: ☒ 20-30  $\mu$ m ☐ OTHER \_\_\_\_\_

**BOARD FINISH:**  
SILKSCREEN: ☒ TOP ☒ BOTTOM  
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER \_\_\_\_\_  
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER \_\_\_\_\_  
☒ MATTE ☐ SEMI-GLOSS

**SURFACE FINISH:** ☒ IMMERSION GOLD (ENIG) ☐ ENEPG  
☐ IM. TIN/SILVER OR EQUIV ☐ OTHER \_\_\_\_\_

**ARRAY/PANEL:** ☒ CUT AND TRIM PER M1 BOARD OUTLINE  
☐ N.C. ROUTE ☐ V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☐ RoHS ☐ OTHER \_\_\_\_\_ PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

**ADDITIONAL REQUIREMENTS:**  
MICROSECTION: ☐ YES ☐ NO  
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER  
☒ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
☒ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
☐ TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE:  
Smart Probe Power Supply

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-010269.PcbDoc

ENGINEER:	Bill. X
-----------	---------

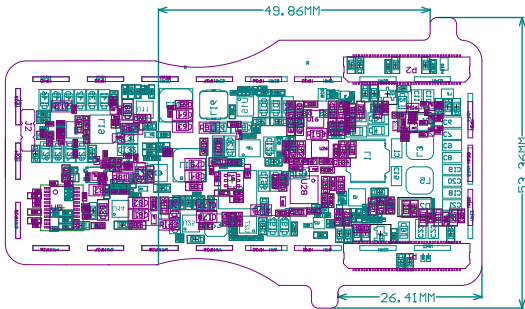
LAYOUT BY:  
Bill.Xu

SCALE: 1.00

ALTUM DESIGNER VERSION  
24.9.1.31



Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	GND1	CF-004	0.69mil		
4	Dielectric 2	PP-006	7.87mil	4.1	
5	Signal 1	CF-004	0.69mil		
6	Dielectric 3	PP-006	7.87mil	4.1	
7	Power 1	CF-004	0.69mil		
8	Dielectric 4	PP-006	7.87mil	4.1	
9	Power 2	CF-004	0.69mil		
10	Dielectric 5	PP-006	7.87mil	4.1	
11	Signal 2	CF-004	0.69mil		
12	Dielectric 6	PP-006	7.87mil	4.1	
13	Layer 1	CF-004	0.69mil		
14	Dielectric 1	FR-4	7.87mil	4.1	
15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. TO THE USER'S NOTICE, THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE INFORMATION CONTAINED HEREIN. THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE INFORMATION CONTAINED HEREIN. THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE INFORMATION CONTAINED HEREIN.

REVISION	00	BOARD	00	DATE	00	DESIGNED BY	00	DATE	00
LAYER NAME	Top Layer	TID #	00	00	00	00	00	00	00
PLT NAME	Top Layer	GENERATED	00	00	00	00	00	00	00

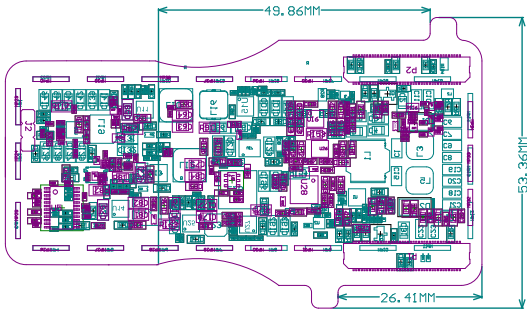
TEXAS INSTRUMENTS (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER
<input checked="" type="checkbox"/> MATTIE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENEPIG	
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	GND1	CF-004	0.69mil		
4	Dielectric 2	PP-006	7.87mil	4.1	
5	Signal 1	CF-004	0.69mil		
6	Dielectric 3	PP-006	7.87mil	4.1	
7	Power 1	CF-004	0.69mil		
8	Dielectric 4	PP-006	7.87mil	4.1	
9	Power 2	CF-004	0.69mil		
10	Dielectric 5	PP-006	7.87mil	4.1	
11	Signal 2	CF-004	0.69mil		
12	Dielectric 6	PP-006	7.87mil	4.1	
13	Layer 1	CF-004	0.69mil		
14	Dielectric 1	FR-4	7.87mil	4.1	
15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				



#### NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. TO THE USER'S NOTICE, THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE BOARD DIMENSIONS. THE USER SHALL VERIFY THE BOARD DIMENSIONS AND THE BOARD LAYER STACK BEFORE PROCEEDING WITH THE BOARD FABRICATION.

REVISION	001	DATE	09/10/2024	DESIGNED BY	Bill Xu
LAYER NAME	Top	TID #	00101010269	QIT	01
PLT FILE	Top	GENERATED	9/10/2024 3:44:02 PM	QIT	01

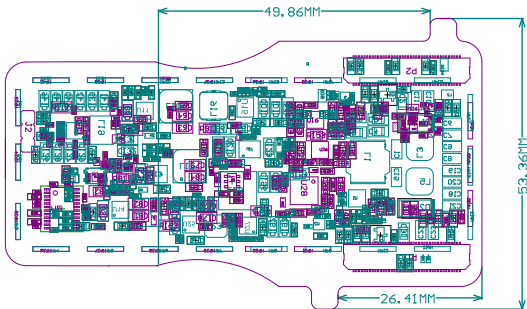
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-	3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTIE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE	
<input checked="" type="checkbox"/> REQUIRED	
<input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:	
Smart Probe Power Supply	
DESIGNED FOR:	
Public Release	
FILE NAME:	
TIDA-010269.PcbDoc	
ENGINEER:	LAYOUT BY:
Bill. Xu	Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION:	
24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	GND1	CF-004	0.69mil		
4	Dielectric 2	PP-006	7.87mil	4.1	
5	Signal 1	CF-004	0.69mil		
6	Dielectric 3	PP-006	7.87mil	4.1	
7	Power 1	CF-004	0.69mil		
8	Dielectric 4	PP-006	7.87mil	4.1	
9	Power 2	CF-004	0.69mil		
10	Dielectric 5	PP-006	7.87mil	4.1	
11	Signal 2	CF-004	0.69mil		
12	Dielectric 6	PP-006	7.87mil	4.1	
13	Layer 1	CF-004	0.69mil		
14	Dielectric 1	FR-4	7.87mil	4.1	
15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				



#### NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. BOARD DIMENSION: 90 MM X 53.36 MM. TID #: 010269. DATE: 9/18/2023. TIME: 3:44:05 PM. TEXAS INSTRUMENTS

REVISION	00	BOARD	010269	DATE	00	SUN 9/18/2023 3:44:05 PM	TEXAS INSTRUMENTS
LAYER NAME	Top	TID #	010269	#	011	mottoB pldmææa æM	
PLT NAME	Assembly Bottom	GENERATED	9/18/2023	3:44:05 PM	mottoB pldmææa æM		

DESIGN INFORMATION		
MIN. TRACK WIDTH:	4 MIL	
MIN. CLEARANCE:	4.25 MIL	
MIN. VIA PAD SIZE:	12 MIL	
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL		
PER IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/-	3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-		3 MIL
MATERIAL:		
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4		
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER	
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-	
DRILLING:		
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER	
BOARD FINISH:		
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH:		
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENERP		
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER		
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:		
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER		
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER		
ADDITIONAL REQUIREMENTS:		
MICROSECTION: <input type="checkbox"/> YES		
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER		
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE		
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE		
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE		
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE		



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

1

2

3

4

5

6

223 ■ These assemblies must be checked for compliance with the following requirements:

224 ■ These assemblies must comply with the following requirements:

225 ■ These assemblies are ESD sensitive and must be observed.

226 ■ Install label in silkscreened box.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	2.76mil	4.2	
1	Top Layer	FR-4	7.87mil	4.1	
2	Dielectric 1	CF-004	0.69mil	4.1	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil	4.1	
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil	4.1	
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil	4.1	
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil	4.1	
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil	4.1	
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer	FR-4	7.87mil	4.1	
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay	Solder Resist	1.00mil	3.5	

49.86MM

53.36MM

26.41MM

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. ASSEMBLY VARIANT: [No Variations]

PCB: 010269

BOARD: 010269

DATE: 01/10/2023

DESIGNER: TI

LAYER NAME = 010269

TID #: 010269

DATE: 01/10/2023

DESIGNER: TI

PLT: 010269

DATE: 01/10/2023

DESIGNER: TI

DATE: 01/10/2023

NOTES: <UNLESS OTHERWISE SPECIFIED>

1.FABRICATE PER IPC-6012A CLASS 2

2.LAMINATE MATERIAL: FR4

3.COPPER WEIGHT: SEE STACKUP

4.BOARD THICKNESS: 1.6MM +/- 10%

5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK

6.SURFACE FINISH: ENIG

7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.

8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.

9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN

10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.

11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.

12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,

13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.

14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.

15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.

16.FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE.

17.FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.

18.FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.

19.BOARD DIMENSION: 90 MM X 53.36 MM.

20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(1.4MIL) AND REMAINING LAYERS WILL BE HALF OUNCE (0.7MIL)

21.ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL

MIN. CLEARANCE: 4.25 MIL

MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

FR-408 FR-4 High Tg OTHER FR-4

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2

OTHER +/-

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2

OTHER +/-

DRILLING:

REFERENCE: AS SHOWN NC\_DRILL FILES

PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:

SILKSCREEN: TOP BOTTOM

SILKSCREEN COLOR: WHITE OTHER

SOLDER RESIST COLOR: GREEN OTHER

MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSSION GOLD (ENG) ENERP

IMM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE

N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

ANSI IPC-A-600F CLASS -> 1 2 3

RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE

TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Probe Power Supply

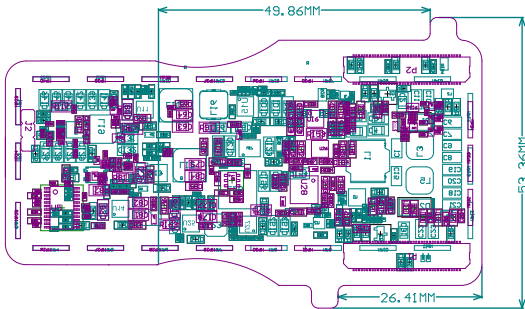
DESIGNED FOR: Public Release

FILE NAME: TIDA-010269.PcbDoc

ENGINEER: Bill. Xu LAYOUT BY: Bill.Xu

SCALE: 1.00 ALTIM DESIGNER VERSION: 24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay	Solder Resist	1.00mil	3.5	
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.38 TOM 01U0H2 '940' 03XRAM 27H3049M03  
ASSEMBLY VARIANT: [No Variations] [noitsreV oM] :TVAIRAU YJ8M322A

REVISION: 00	DATE: 00	SUN 3:44:11 PM	TEXAS INSTRUMENTS
LAYER NAME = Top	TID #: 00000000000000000000	00000000000000000000	00000000000000000000
PLT: 00000000000000000000	00000000000000000000	00000000000000000000	00000000000000000000

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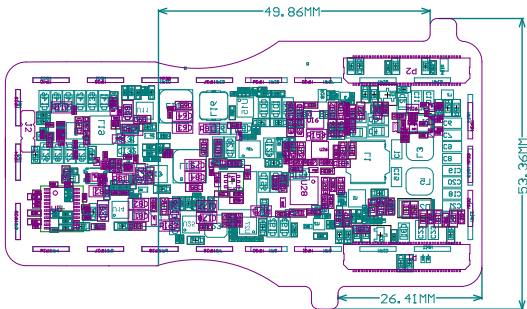
DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-	3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	



Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
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5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
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	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>


- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
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- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
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21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



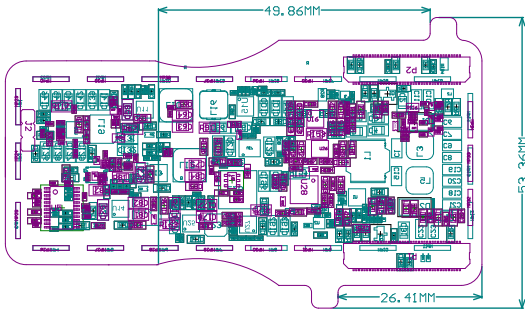
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. TO: 03/04/2024 10:00:00 AM  
ASSEMBLY VARIANT: [No Variations]

DESIGNER: Bill Xu	DATE: 03/04/2024	TIME: 10:00:00 AM	PROJECT: Smart Probe Power Supply
LAYER NAME = Top	TID #: 010269	QIT	03/04/2024 10:00:00 AM
PLTNAME: TID010269.PcbDoc	GENERATED: 03/04/2024 10:00:00 AM	DESIGNED BY: Bill Xu	DESIGNED FOR: Public Release

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DESIGN INFORMATION	
MIN. TRACK WIDTH: 4 MIL MIN. CLEARANCE: 4.25 MIL MIN. VIA PAD SIZE: 12 MIL MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL: <input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4 THICKNESS: <input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-	
DRILLING: REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER	
BOARD FINISH: SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER <input checked="" type="checkbox"/> MATTIE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENERP <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL: <input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF: <input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: <input type="checkbox"/> YES BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER <input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE <input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE <input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
	
PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill Xu	LAYOUT BY: Bill Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
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	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
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- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
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21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.38 TOM DUOH2 '940' 03XRAM 27124049M03  
ASSEMBLY VARIANT: [No Variations] [noitsivU oM] :TVAIRAU YJBM322A

REVISIONS	DATE	DESCRIPTION	BY	APP'D
1	08/01/2024	Initial Release	Bill Xu	
2	08/01/2024	Design Change	Bill Xu	
3	08/01/2024	Final Release	Bill Xu	

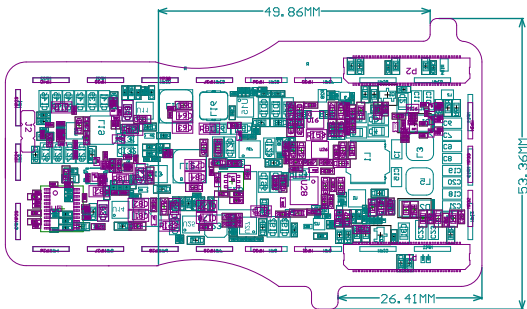
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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER
<input checked="" type="checkbox"/> MATTIE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENERP	
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
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ENGINEER: Bill Xu	LAYOUT BY: Bill Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	1.00mil	3.5	
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15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				



#### NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
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- 3.COPPER WEIGHT: SEE STACKUP
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- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. TO THE USER'S NOTICE, THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE INFORMATION CONTAINED HEREIN. THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE INFORMATION CONTAINED HEREIN. THE DESIGNER IS NOT RESPONSIBLE FOR THE ACCURACY OF THE INFORMATION CONTAINED HEREIN.

REVISIONS	00	BOARD 85010A-010269	DATE: 00	SUN 3/28/2016 10:08:10 AM
LAYER NAME =	Top	TID #: 85010A-010269	# QIT	00000000000000000000
PLT FILE =	85010A-010269	GENERATED: 9/18/2016 10:08:10 AM	3:44:20 PM	TEXAS INSTRUMENTS

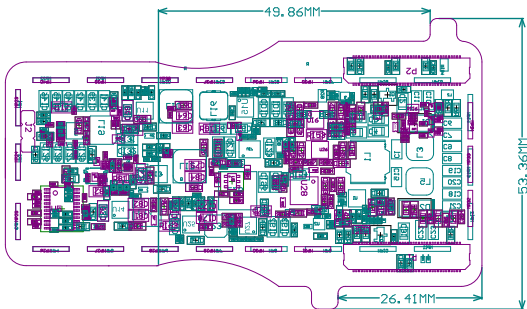
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-	3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. TO DETERMINE WHICH COMPONENTS ARE MARKED 'DNP', SEE THE 'DNP' COLUMN IN THE COMPONENT LIST. ASSEMBLY VARIANT: [No Variations]

PCB: 01010A-010269	00	BOARD: 01010A-010269	00	SUN: 01010A-010269	00
LAYER NAME = 01010A-010269	00	TID #: 01010A-010269	# QIT	01010A-010269	00
PLT: 01010A-010269	00	01010A-010269	00	01010A-010269	00

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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4	
THICKNESS:	62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER
<input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENERP	
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

Z23 ■ These assemblies must be covered by a top solder mask or a top solder mask with an acceptable solder mask coverage.					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED  
ASSEMBLY VARIANT: [No Variations]

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- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ) PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 0.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMASINIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

C

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-010269.PcbDoc

ENGINEER:  
Bill. Xu

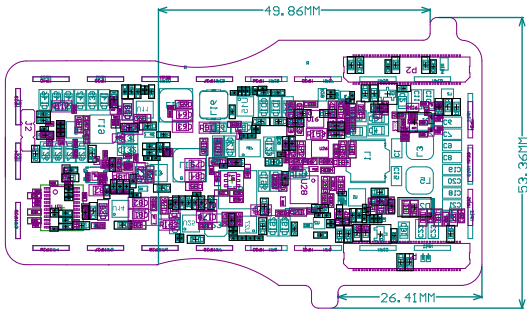
SCALE: 1.00

LAYOUT BY:  
Bill.Xu

ALTUM DESIGNER VERSION:  
24.9.1.31



Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
Top Solder	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
2	Dielectric 1	FR-4	7.87mil	4.2	
3	GND1	CF-004	0.69mil		
4	Dielectric 2	PP-006	7.87mil	4.1	
5	Signal 1	CF-004	0.69mil		
6	Dielectric 3	PP-006	7.87mil	4.1	
7	Power 1	CF-004	0.69mil		
8	Dielectric 4	PP-006	7.87mil	4.1	
9	Power 2	CF-004	0.69mil		
10	Dielectric 5	PP-006	7.87mil	4.1	
11	Signal 2	CF-004	0.69mil		
12	Dielectric 6	PP-006	7.87mil	4.1	
13	Layer 1	CF-004	0.69mil		
14	Dielectric 1	FR-4	7.87mil	4.1	
15	Bottom Layer		2.76mil		
16	Bottom Solder	Solder Resist	1.00mil	3.5	
17	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
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16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38 TOM DUOH2 '940' 03XRAM 27123404M03  
ASSEMBLY VARIANT: [No Variations] [noitsreV oM] :TVAIRAU YJBM322A

PCB: 01010A-010269	00	BOARD: 01010A-010269	00	SUN322A: 01010A-010269
LAYER NAME = 01010A-010269	00	TID #: 01010A-010269	# QIT	01010A-010269
PLT: 01010A-010269	00	GENERATED: 9/18/2024	3:44:28 PM	TEXAS INSTRUMENTS

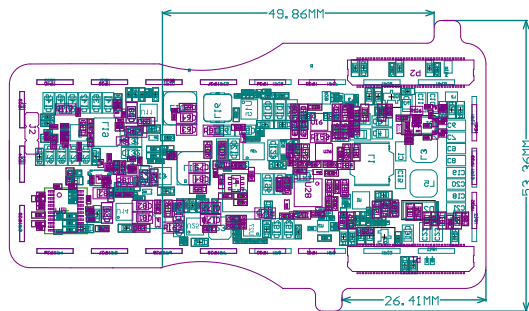
DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/-
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1.00	
ALTIM DESIGNER VERSION: 24.9.1.31	

221 ■ Install label in silkscreened box after final wash. Text shall be 9 pt font. Text shall be per the Label Table in the


- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38  
ASSEMBLY VARIANT: [No Variations]

AGE	AGE	BIRTH DATE	WED	FPOB	ICPN	98DE	00	BOARD	#	SID#	010269	CAREV	00	SUN	REG	NORTH	MORRISON	COOP	60F
LAYER NAME =	N50 300m x 100m x 100m Optom							TID #	EASID#		010269	#	QIT motto@ uidm922af dM						
PLOT NAME	EMBEDDED Cavity SE-PT-							GENERATED	e	#		9/19/2024	33	3:44:32 Private3 belbedTEXAS INSTRUMENTS JA					

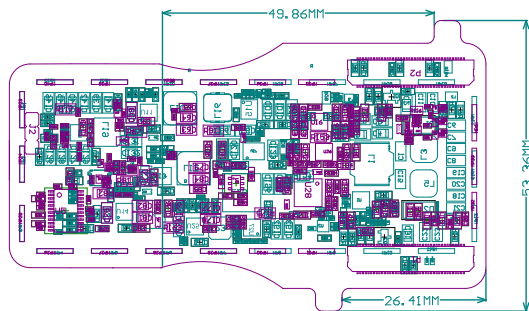
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.75 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4
THICKNESS: <input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10%	<input type="checkbox"/> OTHER _____
TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	<input type="checkbox"/> OTHER +/- _____
BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	<input type="checkbox"/> OTHER +/- _____
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN	<input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um	<input type="checkbox"/> OTHER _____
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP	<input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE	<input type="checkbox"/> OTHER _____
SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN	<input type="checkbox"/> OTHER _____
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG)	
<input type="checkbox"/> IM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER _____
ARRAY/PANEL:	
<input checked="" type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE	<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input checked="" type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input checked="" type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL LAYERS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE:	
Smart Probe Power Supply	
DESIGNED FOR:	
Public Release	
FILE NAME:	
TIDA-010269_PcbDoc	
ENGINEER:	LAYOUT BY:
Bill. Xu	Bill. Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31

Dielectric 4	pp-006	7.8/mil	4.1	
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221 ■ Install label in silkscreened box after final wash. Text shall be 9 pt font. Text shall be per the Label Table in the

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS)  
AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS




A horizontal number line is shown, starting at 0 and ending at 1000 miles. The line is divided into 10 equal segments by vertical tick marks. The first segment, from 0 to 100 miles, is shaded red. Below the line, a double-headed arrow spans the entire length from 0 to 1000 miles, with the text "1000 miles" written below it.

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38  
ASSEMBLY VARIANT: [No Variations]

[illegible]

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.75 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL; HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER FR-4
THICKNESS: <input checked="" type="checkbox"/> 62 MIL (1.6mm) +/- 10%	<input type="checkbox"/> OTHER _____
TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	<input type="checkbox"/> OTHER +/- _____
BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	<input type="checkbox"/> OTHER +/- _____
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN	<input checked="" type="checkbox"/> NC DRILL FILES
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um	<input type="checkbox"/> OTHER _____
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP	<input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE	<input type="checkbox"/> OTHER _____
SOLDER RESIST COLOR: <input checked="" type="checkbox"/> GREEN	<input type="checkbox"/> OTHER _____
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	
<input type="checkbox"/> MM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER _____
ARRAY/PANEL: <input checked="" type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE	<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL MATERIALS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input checked="" type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input checked="" type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
<input type="checkbox"/> TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE:	
Smart Probe Power Supply	
DESIGNED FOR:	
Public Release	
FILE NAME:	
TIDA-010269.PcbDoc	
ENGINEER:	LAYOUT BY:
Bill. Xu	Bill. Xu
SCALE: 1.00	ALTIM DESIGNER VERSION: 24.9.1.31

Z23 ■ These assemblies must be covered with a clear plastic film to protect the components from moisture and corrosion.					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38  
ASSEMBLY VARIANT: [No Variations]

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

- NOTES: (UNLESS OTHERWISE SPECIFIED)
- 1.FABRICATE PER IPC-6012A CLASS 2
  - 2.LAMINATE MATERIAL: FR4
  - 3.COPPER WEIGHT: SEE STACKUP
  - 4.BOARD THICKNESS: 1.6MM +/- 10%
  - 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
  - 6.SURFACE FINISH: ENIG
  - 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
  - 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
  - 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
  - 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
  - 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
  - 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
  - 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
  - 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
  - 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
  16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
  17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
  18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
  19. BOARD DIMENSION: 90 MM X 53.36 MM.
  - 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMASINIG LAYERS WILL BE HALF OUNCE
  21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

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Layer

Name

Material

Thickness

Constant

Board Layer Stack

Top Overlay

Solder Resist

FR-4

1.00mil

3.5

Top Solder

Solder Resist

FR-4

1.00mil

3.5

1

Top Layer

FR-4

2.76mil

4.2

2

Dielectric 1

CF-004

0.69mil

4.1

3

Dielectric 2

PP-006

7.87mil

4.1

4

Signal 1

CF-004

0.69mil

4.1

5

Dielectric 3

PP-006

7.87mil

4.1

6

Power 1

CF-004

0.69mil

4.1

7

Dielectric 4

PP-006

7.87mil

4.1

8

Power 2

CF-004

0.69mil

4.1

9

Dielectric 5

PP-006

7.87mil

4.1

10

Signal 2

CF-004

0.69mil

4.1

11

Dielectric 6

PP-006

7.87mil

4.1

12

Layer 1

CF-004

0.69mil

4.1

13

Dielectric 1

FR-4

7.87mil

4.1

14

Bottom Layer

FR-4

2.76mil

4.1

15

Bottom Solder

Solder Resist

FR-4

1.00mil

3.5

16

Bottom Overlay

Solder Resist

FR-4

1.00mil

3.5

49.86MM

53.36MM

26.41MM

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. ASSEMBLY VARIANT: [No Variations]

PCB LAYER NAME = Top Pad Master

TID #: 202010A-010269

DATE: 9/18/2023

TIME: 3:44:42 PM

PLT FILE: TID010269\_PcbDoc

DESIGNED BY: Bill Xu

DESIGNED FOR: Public Release

FILE NAME: TIDA-010269\_PcbDoc

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NOTES: <UNLESS OTHERWISE SPECIFIED>  
1.FABRICATE PER IPC-6012A CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,  
13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.  
14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.  
15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.  
16. FILL ALL 6MIL , 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE  
17. FILL ALL 6MIL , 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.  
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.  
19. BOARD DIMENSION: 90 MM X 53.36 MM.  
20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE  
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL  
MIN. CLEARANCE: 4.25 MIL  
MIN. VIA PAD SIZE: 12 MIL  
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C  
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL  
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:  
☐ FR-408 ☐ FR-4 High Tg ☒ OTHER FR-4  
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER  
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/-  
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/-

DRILLING:  
REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES  
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:  
SILKSCREEN: ☒ TOP ☒ BOTTOM  
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER  
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER  
☒ MATTIE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENERP  
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☒ CUT AND TRM PER M1 BOARD OUTLINE  
☐ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:  
MICROSECTION: ☐ YES  
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER  
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE:  
Smart Probe Power Supply

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-010269\_PcbDoc

ENGINEER:  
Bill. Xu

LAYOUT BY:  
Bill.Xu

SCALE: 1.00

ALTIM DESIGNER VERSION:  
24.9.1.31




Z23 ■ These assemblies must be covered by a silkscreen label with the following information:					
	Top Solder	Solder Resist	1.00mm	3.5	
1	Top Layer		2.76mm		
2	Dielectric	FR-4	2.87mm	4.2	
3	GND1	CF-004	0.28mm		
4	Dielectric 2	PP-006	2.87mm	4.1	
5	Signal 1	CF-004	0.69mm		
6	Dielectric 3	PP-006	2.87mm	4.1	
7	Power 1	CF-004	0.69mm		
8	Dielectric 4	PP-006	2.87mm	4.1	

1.FABRICATE PER IPC-6012A CLASS 2  
2.LAMINATE MATERIAL: FR4  
3.COPPER WEIGHT: SEE STACKUP  
4.BOARD THICKNESS: 1.6MM +/- 10%  
5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK  
6.SURFACE FINISH: ENIG  
7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.  
8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.  
9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN  
10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.  
11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007" ) PER INCH AS MEASURED PER IPC-TM-650.  
12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPHT AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,

19. BOARD DIMENSION: 90 MM X 53.36 MM.

20. TOP, L6, L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE (PROCESSED THICKNESS) AND REMAINING LAYERS WILL BE HALF OUNCE

21. ALL VIAS ARE TUNED EXCEPT ON PAD VIAS

 <b>TEXAS INSTRUMENTS</b>	
PROJECT TITLE: Smart Probe Power Supply	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010269.PcbDoc	
ENGINEER: Bill. Xu	LAYOUT BY: Bill.Xu
SCALE: 1:00	ALTIM DESIGNER VERSION: 24.9.1.31



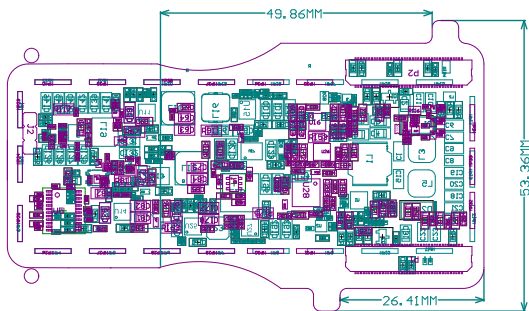
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1	2	3	4	5	6
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Dielectric 4	PP-006	7.8/mil	4.1	
--------------	--------	---------	-----	--

271 ■ Install label in silkscreened box after final wash. Text shall be 9 pt font. Text shall be per the Label Table in the

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10  
TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING  
IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING  
IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C  
COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK.  
SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ) PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPPTH AND FIDUCIALS.  
VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED  
MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 0.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER.  
THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE(PROCESSED THICKNESS)  
AND REMASINIG LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. 38  
ASSEMBLY VARIANT: [No Variations]

[illegible]

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**DESIGN INFORMATION**

MIN. TRACK WIDTH: 4 MIL  
MIN. CLEARANCE: 4.75 MIL  
MIN. VIA PAD SIZE: 12 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: 2x2 5 MIL, HOLES +/- 3 MIL  
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408 ☐ FR-4 High Tg ☒ OTHER FR-4

THICKNESS: ☒ 62 MIL (1.6mm) +/- 10% ☐ OTHER \_\_\_\_\_

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

DRLING:

REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30  $\mu$ m ☐ OTHER \_\_\_\_\_

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER \_\_\_\_\_

SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER \_\_\_\_\_  
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENIEPG  
☐ MM. TIN/SILVER OR EQUIV ☐ OTHER \_\_\_\_\_

ARRAY/PANEL: ☒ CUT AND TRIM PER M1 BOARD OUTLINE  
☐ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☐ RoHS ☐ OTHER \_\_\_\_\_ PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☒ YES

BASE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☒ XX MIL VAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
☐ XX MIL VAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

PROJECT TITLE:  
Smart Probe Power Supply

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-010269.PcbDoc

ENGINEER:	Bill. X
-----------	---------

LAYOUT BY:  
Bill.Xu

SCALE: 1.00

ALTUM DESIGNER VERSION  
24.9.1.31

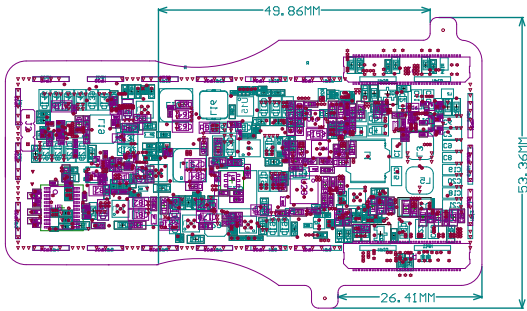
Layer	Name	Material	Thickness	Constant	Board Layer Stack
Top Overlay	Top Overlay	Solder Resist	1.00mil	3.5	
1	Top Layer	FR-4	2.76mil	4.2	
2	Dielectric 1	CF-004	0.69mil	4.1	
3	Dielectric 2	PP-006	7.87mil	4.1	
4	Signal 1	CF-004	0.69mil	4.1	
5	Dielectric 3	PP-006	7.87mil	4.1	
6	Power 1	CF-004	0.69mil	4.1	
7	Dielectric 4	PP-006	7.87mil	4.1	
8	Power 2	CF-004	0.69mil	4.1	
9	Dielectric 5	PP-006	7.87mil	4.1	
10	Signal 2	CF-004	0.69mil	4.1	
11	Dielectric 6	PP-006	7.87mil	4.1	
12	Layer 1	CF-004	0.69mil	4.1	
13	Dielectric 1	FR-4	7.87mil	4.1	
14	Bottom Layer	FR-4	2.76mil	4.2	
15	Bottom Solder	Solder Resist	1.00mil	3.5	
16	Bottom Overlay	Solder Resist	1.00mil	3.5	

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair
⊕	8	5.91mil (0.150mm)	PTH	Round	Top Layer - Bottom Layer
⊙	298	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer
◇	1	8.27mil (0.210mm)	PTH	Round	Top Layer - Bottom Layer
⊗	37	8.66mil (0.220mm)	PTH	Round	Top Layer - Bottom Layer
⊕	336	9.84mil (0.250mm)	PTH	Round	Top Layer - Bottom Layer
▽	288	11.81mil (0.300mm)	PTH	Round	Top Layer - Bottom Layer
□	1	19.69mil (0.500mm)	PTH	Round	Top Layer - Bottom Layer
▽	2	31.50mil (0.800mm)	PTH	Round	Top Layer - Bottom Layer
□	3	35.43mil (0.900mm)	PTH	Round	Top Layer - Bottom Layer
⊙	2	120.89mil (3.048mm)	NPTH	Round	Top Layer - Bottom Layer
	976 Total				

Tolerance:  
For 6 Mil +0/-6 Mil

#### NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR: GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
- 13.100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED.
- 14.LOCAL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED. THIS DOCUMENT IS FOR INFORMATION ONLY. NO WARRANTIES ARE MADE BY TEXAS INSTRUMENTS FOR THIS DOCUMENT.

DESIGNER: Bill Xu	DATE: 01/01/2024	REV: 00	BOARD: 0101010269	DATE: 01/01/2024	REV: 00	SUN: 01/01/2024	TIME: 10:00:00	FILE: 0101010269
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PLT: 0101010269	0101010269	0101010269	0101010269	0101010269	0101010269	0101010269	0101010269	0101010269

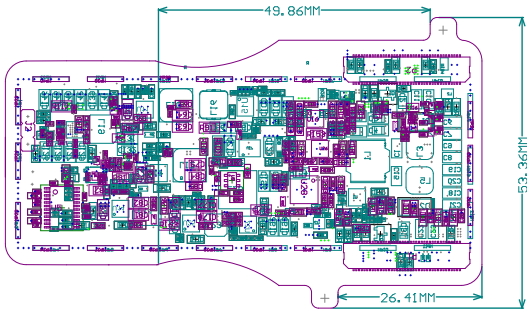
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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/-
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94-V0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:	Smart Probe Power Supply
DESIGNED FOR:	Public Release
FILE NAME:	TIDA-010269.PcbDoc
ENGINEER:	Bill Xu
LAYOUT BY:	Bill Xu
SCALE:	1.00
ALTIM DESIGNER VERSION:	24.9.1.31

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		2.76mil		
	Dielectric 1	FR-4	7.87mil	4.2	
2	GND1	CF-004	0.69mil		
	Dielectric 2	PP-006	7.87mil	4.1	
3	Signal 1	CF-004	0.69mil		
	Dielectric 3	PP-006	7.87mil	4.1	
4	Power 1	CF-004	0.69mil		
	Dielectric 4	PP-006	7.87mil	4.1	
5	Power 2	CF-004	0.69mil		
	Dielectric 5	PP-006	7.87mil	4.1	
6	Signal 2	CF-004	0.69mil		
	Dielectric 6	PP-006	7.87mil	4.1	
7	Layer 1	CF-004	0.69mil		
	Dielectric 1	FR-4	7.87mil	4.1	
8	Bottom Layer		2.76mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				



NOTES: <UNLESS OTHERWISE SPECIFIED>

- 1.FABRICATE PER IPC-6012A CLASS 2
- 2.LAMINATE MATERIAL: FR4
- 3.COPPER WEIGHT: SEE STACKUP
- 4.BOARD THICKNESS: 1.6MM +/- 10%
- 5.NO OF LAYERS: 12 AS PER SUPPLIED ARTWORK
- 6.SURFACE FINISH: ENIG
- 7.SINGLE ENDED TRACES WITH 7MILS WIDTH IN LAYERS 1,12 AND 4MILS WIDTH IN LAYERS 3,5,8 & 10 TO BE 50 OHM +/- 10% IMPEDANCE CONTROLLED.
- 8.DIFFERENTIAL TRACES WITH 5MILS WIDTH AND 6MILS SPACING IN LAYERS 1,12 AND 4MILS WIDTH AND 7MILS SPACING IN LAYERS 3,5 & 10 TO BE 100 OHM +/- 10% IMPEDANCE CONTROLLED.
- 9.SOLDERMASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C COLOR:GREEN
- 10.SILKSCREEN: BOTH SIDE WITH PERMANENT NON CONDUCTIVE WHITE EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERED ENTITY.
- 11.BOW AND TWIST NOT TO EXCEED 0.180MM (0.007 ") PER INCH AS MEASURED PER IPC-TM-650.
- 12.SOLDER MASK CLEARANCE IS GIVEN SAME AS PAD SIZE EXCEPT FOR NPTH AND FIDUCIALS. VENDOR SHALL OVERSIZE THE MASK CLEARANCES AS PER THE REQUIRED MANUFACTURING CAPABILITIES,
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- 14.ALL INNER LAYER UNCONNECTED PADS SHALL BE REMOVED.
- 15.LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.
16. FILL ALL 6MIL, 8.02MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE TOP SIDE
17. FILL ALL 6MIL, 8.03MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON THE BOTTOM SIDE.
18. FILL ALL 8.01MIL VIAS WITH CONDUCTIVE EPOXY PLATED OVER WITH COPPER. THE SURFACE SHOULD BE FLAT ON BOTH TOP AND BOTTOM SIDE.
19. BOARD DIMENSION: 90 MM X 53.36 MM.
- 20.TOP,L6,L7 AND BOTTOM COPPER THICKNESS IS 1 OUNCE<PROCESSED THICKNESS> AND REMAINING LAYERS WILL BE HALF OUNCE
21. ALL VIAS ARE TENTED EXCEPT ON PAD VIAS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.38 TOM 01U0H2 '94M' 03XRAM 27H304QMOJ  
ASSEMBLY VARIANT: [No Variations] [noitsivU oM] :TVAIRAU YJBM322A

PCB: 010269	00	BOARD: 010269	00	SUN 3/28/2018 10:51:00 AM
LAYER NAME = 010269	00	TID #: 010269	00	010269
PLT: 010269	00	010269	00	010269

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DESIGN INFORMATION	
MIN. TRACK WIDTH:	4 MIL
MIN. CLEARANCE:	4.25 MIL
MIN. VIA PAD SIZE:	12 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/-	5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/-	3 MIL
MATERIAL:	
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg
<input checked="" type="checkbox"/> OTHER	FR-4
THICKNESS:	62 MIL (1.6mm) +/-10%
<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	
<input type="checkbox"/> OTHER +/-	
BOW & TWIST:	ANSI IPC-6012 TYPE 3 CLASS 2
<input type="checkbox"/> OTHER +/-	
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN
<input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS:	20-30 um
<input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP
<input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE
<input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN
<input type="checkbox"/> OTHER	
<input checked="" type="checkbox"/> MATTE	<input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	<input checked="" type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1
<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE
<input checked="" type="checkbox"/> REQUIRED	<input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



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